Remarks

As stated above, the applicant appreciates the examiner's thorough examination of the subject application and requests reexamination and reconsideration of the subject application in view of the following amendments and remarks.

Concerning Item 1 of the subject action, the Examiner objects to claim 2 due to a typographical error. In response to this objection, the applicant has amended claim 2 to address this error. Additionally, applicant has amended claims 20 & 22 to correct additional typographical errors.

Concerning Items 2-20, the Examiner rejects claims 1-26, under 35 USC §103(a), based on the combination of the teachings of Miyazawa (i.e., U.S. Patent No.: 5,907,682; hereinafter Miyazawa) and Wolf et al (U.S. Patent No.: 6,526,069; hereinafter Wolf).

Of the rejected claims, claims 1, 10, 14, 15, 17, 18 and 20 are independent claims and claims 2-9, 11-13, 16, 19 and 21-26 are dependent claims.

Concerning original claim 1, applicants claim:

> 1. (Original) A temporary storage device, comprising: a first buffer, the first buffer configured to receive information, the information provided in association with a line clock signal, the **first buffer configured to receive a first write enable signal for storing a first portion of the information**; a second buffer, the second buffer configured to receive the information, the information provided in association with the line clock signal, **the second buffer configured to receive a second write enable signal for storing a second portion of the information different from the first portion of the information**; a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information; and a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor have a third buffer for storing the first portion of the information. *Emphasis Added.*

Concerning currently amended claim 10, applicants claim:

> 10. (Currently Amended) A network node comprising: a receive line interface configured to receive at least one transmission; **buffers** configured to decouple a line clock signal from input data and to couple a system clock signal to first and second output data; and a pointer core coupled to receive the first output data from a first buffer of the buffers synchronous to the system clock signal, the pointer core having a pointer core associated buffer configured for synchronous

operation with the system clock signal on an input and an output side; **wherein the buffers include: a first buffer configured to receive a first portion of the input data; and a second buffer configured to receive a second portion of the input data that is different from the first portion**. *Emphasis Added.*

Concerning currently amended claim 14, applicants claim:

14. (Currently Amended) A network node comprising: a frame timing generator, the frame timing generator configured for synchronous operation off of a system clock signal; a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple the system clock signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal, the data outputted from the temporary storage device synchronous to the line clock signal; and a pointer core having a buffer, the buffer configured to receive the data output from the temporary storage device, the buffer configured to operate on both an input side and an output side synchronous with the line clock signal, **wherein the temporary storage device includes: a first buffer configured to receive a first portion of the data output from the frame timing generator; and a second buffer configured to receive a second portion of the data output from the frame timing generator that is different from the first portion**. *Emphasis Added.*

Concerning currently amended claim 15, applicants claim:

15. (Currently Amended) A network comprising: a first network node; a second network node; a communication link for putting the first network node in communication with the second network node; the first network node configured with a receive buffer, the receive buffer comprising: a first buffer, the **first buffer configured to receive at least a first portion of the overhead information**, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store a first portion of the at least a first portion of the overhead information; and a second buffer, the **second buffer configured to receive at least a second portion of the overhead information**, the at least a second portion of the overhead information provided in association with a line clock signal, the second buffer configured to store a second portion of the at least a second portion of the overhead information, **wherein the second portion of the overhead information is different from the first portion of the overhead information**. *Emphasis Added.*

Concerning original claim 17, applicants claim:

17. (Original) A method for avoiding one or more asynchronicities in pointer processing, comprising: providing a first buffer and a second buffer; providing a

frame structure clocked to a line clock to the first buffer; providing the frame structure clocked to the line clock to the second buffer; **storing a first portion of the frame structure in the first buffer**; **storing a second portion of the frame structure in the second buffer, the second portion different from the first portion**; clocking out the first portion of the frame structure from the first buffer synchronous to a system clock signal; clocking out the second portion of the frame structure from the second buffer synchronous to the system clock signal; providing the first portion and the second portion of the frame structure from the first buffer and the second buffer to a pointer processor buffer; and clocking out with a pulse signal synchronized with the system clock signal the first portion and the second portion of the frame structure from the pointer processor buffer. *Emphasis Added.*

Concerning currently amended claim 18, applicants claim:

18. (Currently Amended) A network comprising: a first network node; a second network node; a communication link for putting the first network node in communication with the second network node; the first network node configured with a receive buffer and a transmit buffer, the transmit buffer comprising: a frame timing generator; and a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple a system clock signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal and outputted from the temporary storage device synchronous to the line clock signal; **wherein the temporary storage device includes: a first buffer configured to receive a first portion of the data output from the frame timing generator; and a second buffer configured to receive a second portion of the data output from the frame timing generator that is different from the first portion**. *Emphasis Added.*

Concerning currently amended claim 20, applicants claim:

20. (Currently Amended) A temporary storage device configured to receive overhead information and data, comprising: a first buffer, the **first buffer coupled to receive at least a first portion of the overhead information**, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store the at least a first portion of the overhead information to provide first stored overhead information; a second buffer, the **second buffer coupled to receive at least a second portion of the overhead information**, the at least a second portion of the overhead information provided in association with the line clock signal, the second buffer configured to store the at least a second portion of the overhead information to provide second stored overhead information; and the first buffer and the second buffer coupled to receive a system clock signal and configured to respectively clock out the first

> and second stored information synchronous to the system clock signal, **wherein the second portion of the overhead information is different from the first portion of the overhead information**. *Emphasis Added.*

Concerning the "first buffer" and the "second buffer" of claims 1, 10, 14, 15, 17, 18 and 20, the Examiner states that (with respect to Miyazawa) "Registers (sic) A can be considered as the first buffer and Register B can be considered as the second buffer. Most certainly each register will contain different overhead information from one another based on the desired task to be accomplished" In support of this assertion, the Examiner relies upon column 14, lines 19-34 of Miyazawa. Specifically, the passage replied upon by the Examiner discloses:

> As shown by a broken line in FIG. 14, the receiving processor 4 comprises a program counter 4-1 for holding an address in which an instruction to be executed succeedingly to an instruction which is being executed presently is stored, a program RAM 4-2 for outputting said instruction stored in said address which is held by said program counter 4-1, an instruction register 4-3 for holding said instruction output from said program RAM 4-2, an instruction decoder 4-4 for decoding said instruction held by said instruction register 4-3, a selector 4-5 for selecting output from said reception overhead memory section 3, registers 4-6 and 4-7 for holding data selected by said selector 4-5, and an ALU 4-8 for executing various processes of data input according to a control signal from the instruction decoder 4-4 and stored in registers 4-6 and 4-7, and then outputting the result thereof to the status register 5 and the like. *See Miyazawa, column 14, lines 19-24.*

With respect to the relied-upon Miyazawa passage, the passage merely states that "registers 4-6 and 4-7" are "for holding data selected by said selector 4-5" and fails to disclose (or allude to) the assertion that "[m]ost certainly each register will contain different overhead information from one another based on the desired task to be accomplished" (as asserted by the Examiner).

Accordingly, applicants respectfully assert that the combination of Miyazawa and Wolf is not a proper basis for a 35 USC §103(a) rejection, as the combination of the references fail to disclose each and every element of the applicants' claimed invention.

Therefore, applicant respectfully asserts that independent claims 1, 10, 14, 15, 17, 18 and 20 are patentable over the combination of the Miyazawa and Wolf references. Further, as dependent claims 2-9 depend (either directly or indirectly) upon independent claim 1 (an

allowable base claim), applicant respectfully asserts that dependent claims 2-9 are also patentable over the cited combination of references. As dependent claims 11-13 depend (either directly or indirectly) upon independent claim 10 (an allowable base claim), applicant respectfully asserts that dependent claims 11-13 are also patentable over the cited combination of references. As dependent claim 16 directly depends upon independent claim 15 (an allowable base claim), applicant respectfully asserts that dependent claim 16 is patentable over the cited combination of references. As dependent claim 19 directly depends upon independent claim 18 (an allowable base claim), applicant respectfully asserts that dependent claim 19 is patentable over the cited combination of references. As dependent claims 21-26 depend (either directly or indirectly) upon independent claim 20 (an allowable base claim), applicant respectfully asserts that dependent claims 21-26 are patentable over the cited combination of references.

No new matter is added by these amendments. The applicant respectfully asserts that the subject application is now in condition for allowance. Please apply any charges or credits to deposit account 50-2121.

Respectfully submitted,

Ang et al.

By their Representatives,

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